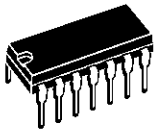
LOW POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

- LOW POWER CONSUMPTION : SPECIAL CMOS OSCILLATOR CONFIGURATION
- MONOSTABLE (one - shot) OR ASTABLE (free-running) OPERATION
- TRUE AND COMPLEMENTED BUFFERED OUTPUTS
- ONLY ONE EXTERNAL R AND C REQUIRED
- BUFFERED INPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

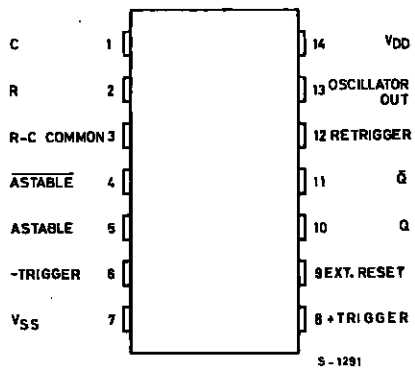
ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4047	

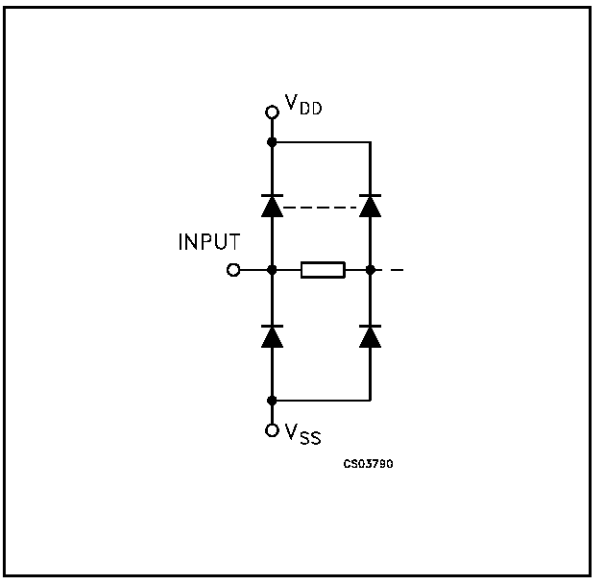
DESCRIPTION

The CC4047 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The CC4047 consist of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$ and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.
For operating modes see functional terminal connections and application notes.

PIN CONNECTION



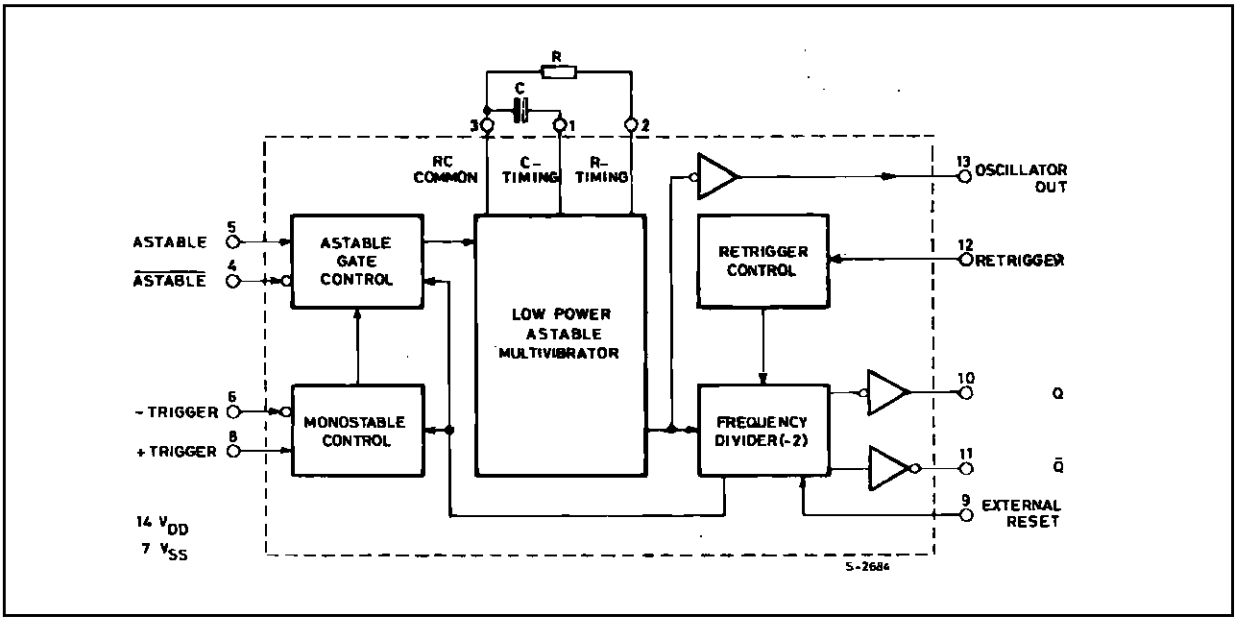
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	C	External Capacitor
2	R	External Resistor
3	RC COM-MON	External Connection to (1) and (2)
4	$\overline{\text{ASTABLE}}$	Complement Astable Pulse
5	ASTABLE	True Astable Pulse
6	-TRIGGER	Negative Trigger Pulse
8	+TRIGGER	Positive Trigger Pulse
9	EXT. RESET	External Reset
12	RETRIG-GER	Retrigger Mode Pulse
13	OSC. OUT	Oscillator Output
10,11	Q, $\overline{Q}$	Q Outputs
7	V_{SS}	Negative Supply Voltage
14	V_{DD}	Positive Supply Voltage

BLOCK DIAGRAM

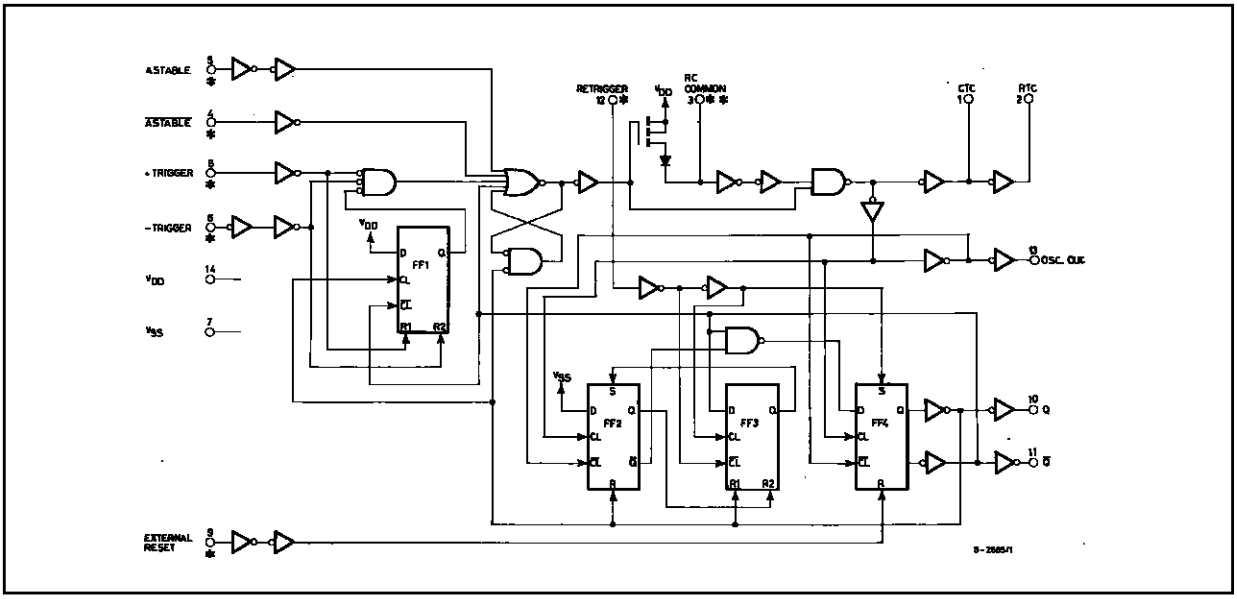


FUNCTIONAL TERMINAL CONNECTIONS

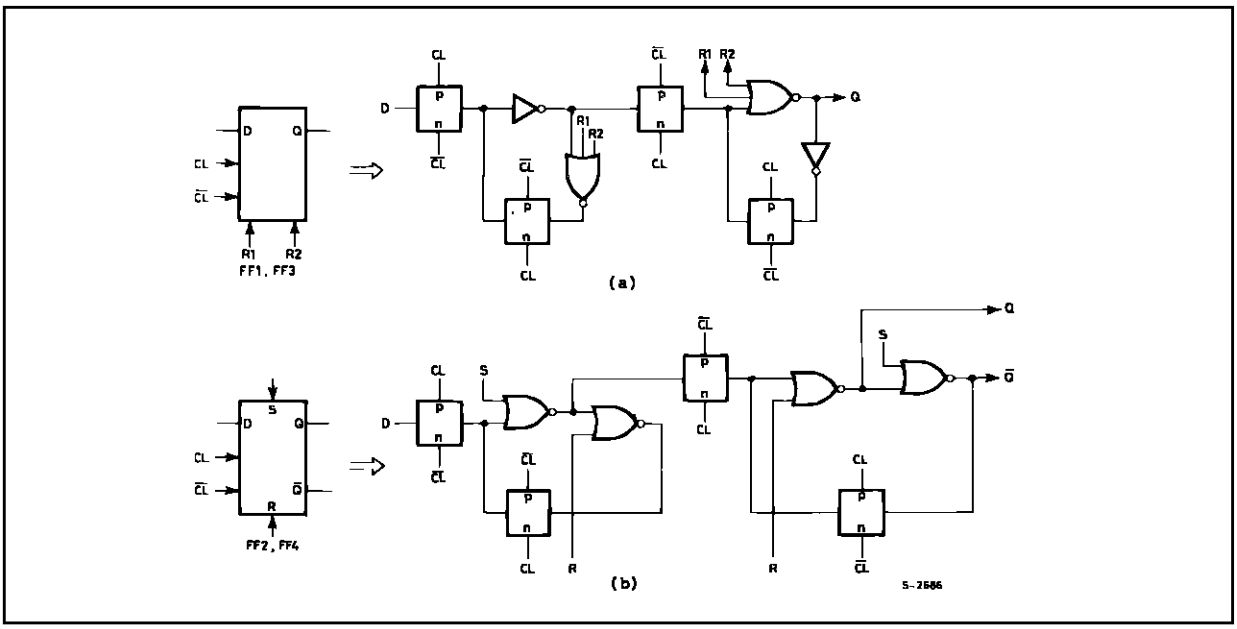
FUNCTION*	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	to V_{DD}	to V_{SS}	Input Pulse to		
Astable Multivibrator					
Free Running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	t_A (10,11) = 4.40RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	t_A (13) = 2.20RC
Monostable Multivibrator					
Positive - Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative - Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10,11) = 2.48RC
External Countdown**	14	5, 6, 7, 8, 9, 12	-	10, 11	

* In all cases external capacitor and resistor between pins, 1, 2 and 3 (see logic diagrams).
** Input pulse to Reset of External Counting Chip.
External Counting Chip Output to pin 4.

LOGIC DIAGRAM



DETAIL FOR FLIP-FLOPS FF1 AND FF3 (a) AND FOR FLIP-FLOPS FF2 AND FF4 (b)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.01	1		30		30	μA
		0/10			10		0.01	2		60		60	
		0/15			15		0.01	4		120		120	
		0/18			18		0.02	20		600		600	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V