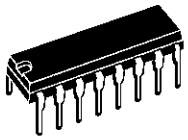
SYNCHRONOUS PARALLEL OR SERIAL IN/SERIAL OUT 8 - STAGE STATIC SHIFT REGISTER

- MEDIUM SPEED OPERATION : 12 MHz (Typ.) At V_{DD} = 10V
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING AND CONTROL GATING
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

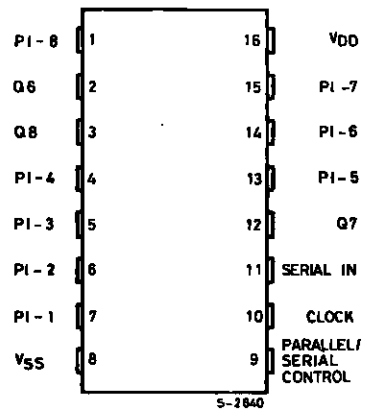
ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4014	

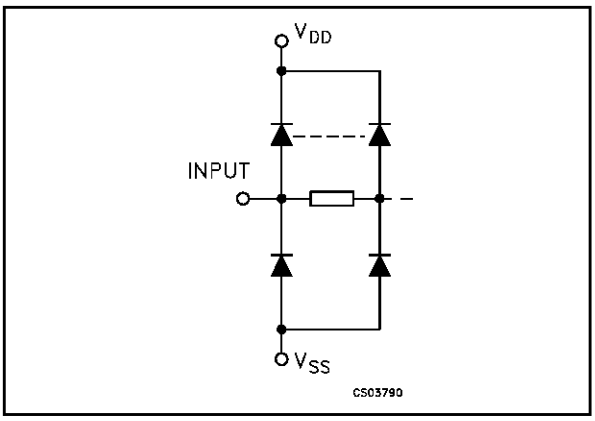
DESCRIPTION

The CC4014 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. This device is an 8-stage parallel or serial input/ serial output register having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop in addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition. In this device, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of he clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

PIN CONNECTION



IINPUT EQUIVALENT CIRCUIT



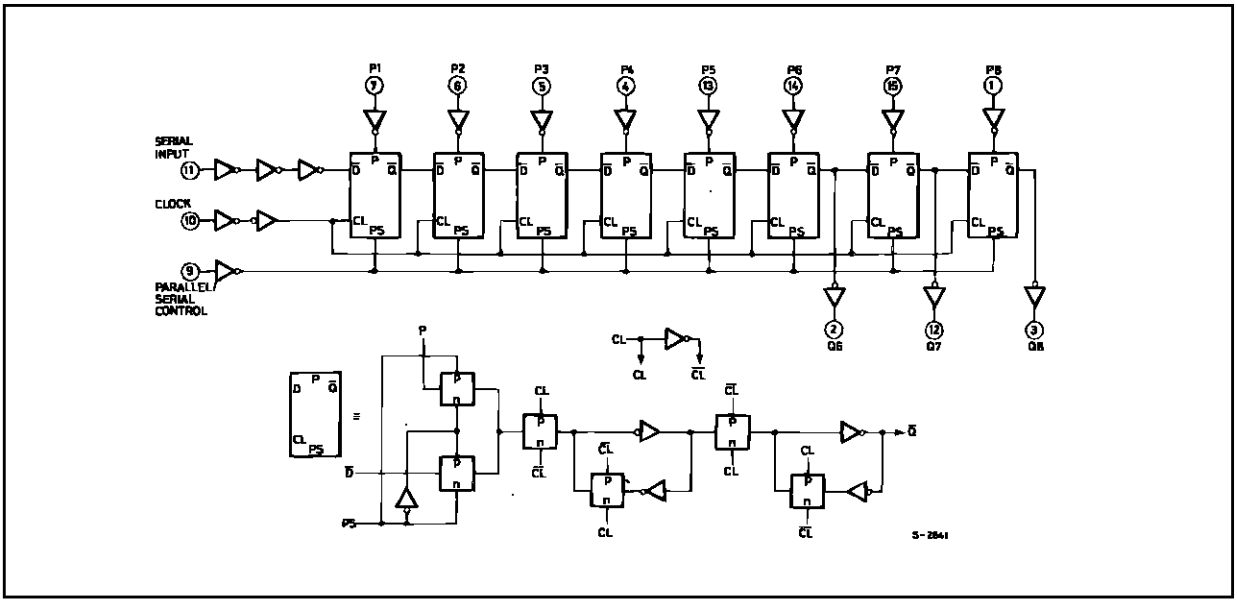
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
7, 6, 5, 4, 13, 14, 15, 1	PI1 to PI8	Parallel Input
11	SERIAL IN	Serial Input
9	PARALLEL/ SERIAL CONTROL	Parallel/Serial Input Control
10	CLOCK	Clock Input
2, 3, 12	Q6, Q7, Q8	Buffered Outputs
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

TRUTH TABLE

CLOCK	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI - 1	PI - n	Q_1 (INTERNAL)	Q_n
⌐¬	X	1	0	0	0	0
⌐¬	X	1	1	0	1	0
⌐¬	X	1	0	1	0	1
⌐¬	X	1	1	1	1	1
⌐¬	0	0	X	X	0	$Q_n - 1$
⌐¬	1	0	X	X	1	$Q_n - 1$
¬⌐	X	X	X	X	Q_1	Q_n

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 1 8	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/18			18		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time	5			160	320	ns
		10			80	160	
		15			60	120	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{CL} (1)	Maximum Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8.5	17		
t_W	Clock Pulse Width	5		180	90		ns
		10		80	40		
		15		50	25		
t_r , t_f	Clock Input Rise or Fall Time	5				15	µs
		10				15	
		15				15	
t_{setup}	Setup Time, serial Input (ref to CL)	5		120	60		ns
		10		80	40		
		15		60	30		
t_{setup}	Setup Time, Parallel Inputs (ref to CL)	5		80	40		ns
		10		50	25		
		15		40	20		
t_{setup}	Setup Time, Parallel/Serial Control (ref to CL)	5		180	90		ns
		10		80	40		
		15		60	30		
t_{hold}	Hold Time, serial in, parallel in, parallel /serial control	5		0			ns
		10		0			
		15		0			

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage of the estimated capacitive load.