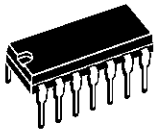
DUAL D-TYPE FLIP FLOP

- SET - RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM SPEED OPERATION 16MHz (TYP.) CLOCK TOGGLE RATE AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

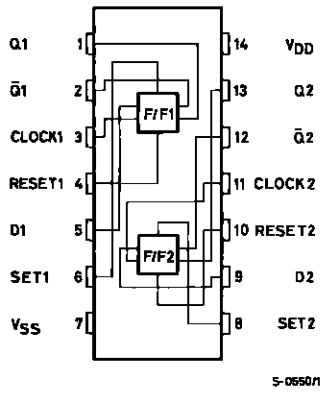
ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4013	

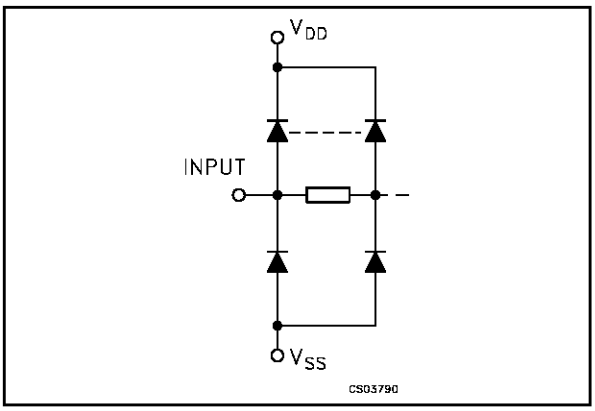
DESCRIPTION

The CC4013 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The CC4013 consists of two identical, independent data type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. This device can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the $\overline{Q}$ output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively

PIN CONNECTION



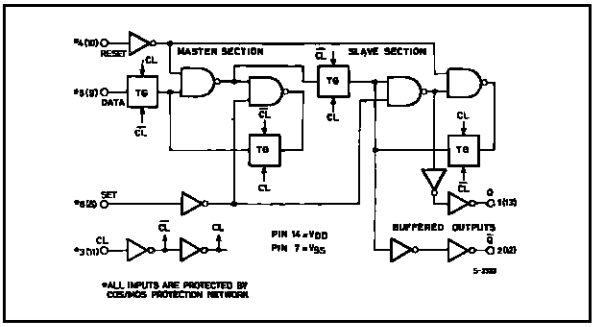
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 11	CLOCK1 CLOCK2	Clock Inputs
4, 10	RESET1 RESET2	Reset Inputs
6, 8	SET1, SET2	Set Inputs
5, 9	D1, D2	Data Inputs
1, 13	Q1, Q2	Data Outputs
2, 12	$\overline{Q1}$, $\overline{Q2}$	Data Outputs
7	V_{SS}	Negative Supply Voltage
14	V_{DD}	Positive Supply Voltage

LOGIC DIAGRAM



TRUTH TABLE

CLOCK$^{\Delta}$	D	RESET	SET	Q	$\overline{Q}$
⌐¬	L	L	L	L	H
⌐¬	H	L	L	H	L
¬⌐	X	L	L	Q	$\overline{Q}$
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X : Don't Care
$^{\Delta}$: Low Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 1 8	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.02	1		30		30	μA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/18			18		0.04	20		600		600	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

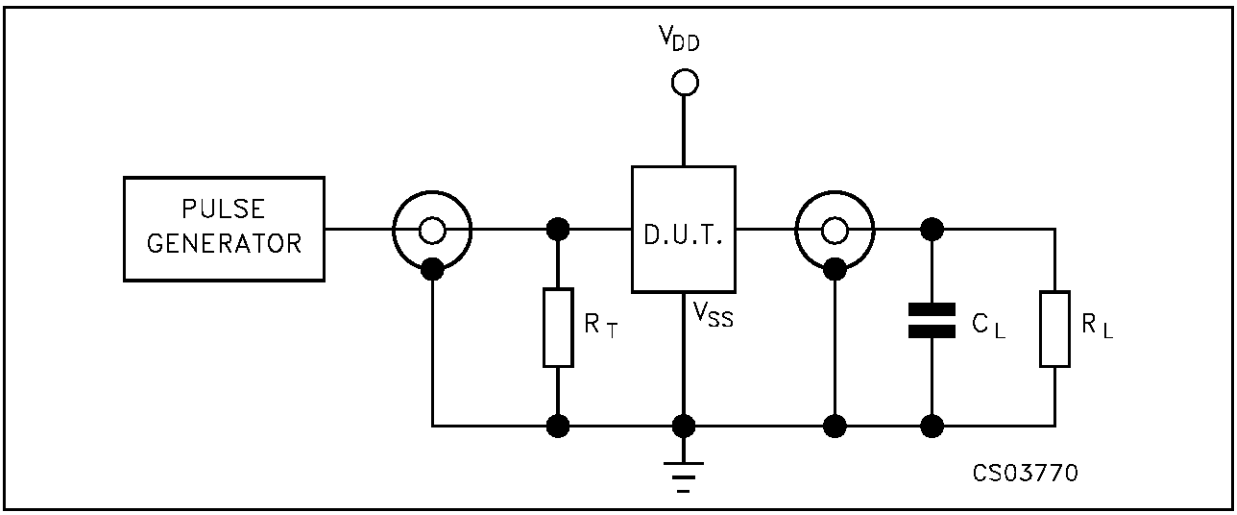
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Propagation Delay Time (CLOCK to Q or $\overline{Q}$ outputs)	5			150	300	ns
		10			65	130	
		15			45	90	
t_{PLH}	Propagation Delay Time (SET to Q or RESET to $\overline{Q}$)	5			150	300	ns
		10			65	130	
		15			45	90	
t_{PHL}	Propagation Delay Time(SET to $\overline{Q}$ or RESET to Q)	5			200	400	ns
		10			85	170	
		15			60	120	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{CL} (1)	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		8	16		
		15		12	24		
t_W	Clock Pulse Width	5		140	70		ns
		10		60	30		
		15		40	20		
t_r , t_f (2)	Clock Input Rise or Fall Time	5				15	µs
		10				4	
		15				1	
t_W	Set or Reset Pulse Width	5		180	90		ns
		10		80	40		
		15		50	25		
t_{setup}	Data Setup Time	5		40	20		ns
		10		20	10		
		15		15	7		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) Input tr, tf = 5ns
(2) If more than unit is cascaded in a parallel clocked application, tr should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the carry output driving stage for the estimated capacitive load.

TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : CLOCK TO Qn, $\overline{Q}$n PROPAGATION DELAY TIMES, Dn TO CLOCK SETUP AND HOLD TIMES, CLOCK MINIMUM PULSE WITDH, MAXIMUM CLOCK FREQUENCY

(f=1MHz; 50% duty cycle)