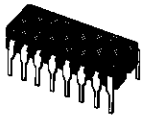
QUAD LOW-TO-HIGH VOLTAGE LEVEL SHIFTER

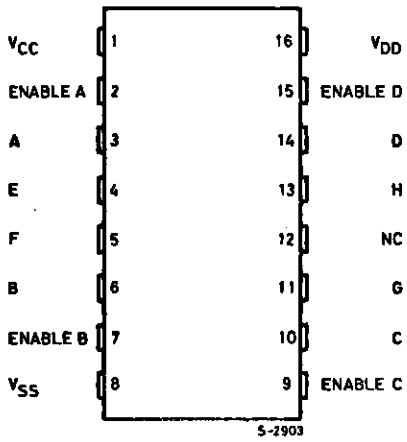
- INDEPENDENCE OF POWER SUPPLY SEQUENCE CONSIDERATIONS – V_{CC} CAN EXCEED V_{DD}, INPUT SIGNALS CAN EXCEED BOTH V_{CC} AND V_{DD}
- UP AND DOWN LEVEL-SHIFTING CAPABILITY
- THREE-STATE OUTPUTS WITH SEPARATE ENABLE CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

DESCRIPTION

The **CC40109** (extended temperature range) and **CC40109** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage. The **CC40109** contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}. The **CC40109**, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, there are no restrictions on the relative magnitudes od the supply voltages or input signals within the device maximum ratings ; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC}, and V_{DD}. When operated in the mode V_{CC} V_{DD}, the **CC40109**, will operate as a high-to-low level-shifter. The **CC40109** also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

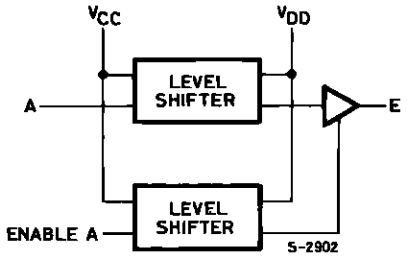


PIN CONNECTIONS



FUNCTIONAL DIAGRAM

1 of 4 units



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage :	– 0.5 to + 18	V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature :	– 55 to + 125	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

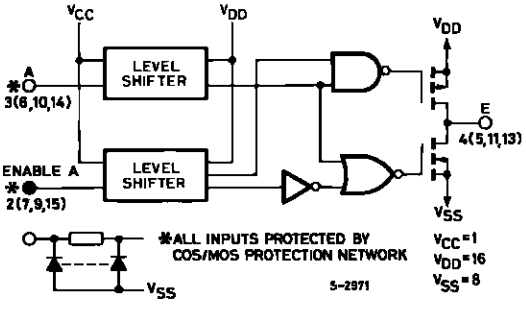
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage are with respect to V_{SS} (GND).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage :	3 to 18	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature :	– 55 to + 125	°C °

LOGIC DIAGRAM



TRUTH TABLE

Mode	Inputs		Outputs
	A, B, C, D	Enable A, B, C, D	E, F, G, H
Low to High Level Shift	0	1	0
	1	1	1
	X	0	Z

LOGIC 0 = LOW (V_{SS}) X = Don't Care. Z = High Impedance.

LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter	Test Conditions					Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{CC} (V)	V_{DD} (V)	T_{Low}* Min	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent Current	0/ 5				5		1		0.02	1		30	μA
		0/10				10		2		0.02	2		60	
		0/15				15		4		0.02	4		120	
		0/18				18		20		0.04	20		600	
V_{OH}	Output High Voltage	0/ 5		< 1		5	4.95		4.95			4.95		V
		0/10		< 1		10	9.95		9.95			9.95		
		0/15		< 1		15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1		5		0.05			0.05		0.05	V
		10/0		< 1		10		0.05			0.05		0.05	
		15/0		< 1		15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		1/9	< 1	5	10	3.5		3.5			3.5		V
			1.5/13.5	< 1	10	15	7		7			7		
V_{IL}	Input Low Voltage		1/9	< 1	5	10		1.5			1.5		1.5	V
			1.5/13.5	< 1	10	15		3			3		3	
I_{OH}	Output Drive Current	0/ 5	2.5			5	– 2		– 1.6	– 3.2		– 1.15		mA
		0/ 5	4.6			5	– 0.64		– 0.51	– 1		– 0.36		
		0/10	9.5			10	– 1.6		– 1.3	– 2.6		– 0.9		
		0/15	13.5			15	– 4.2		– 3.4	– 6.8		– 2.4		
I_{OL}	Output Sink Current	0/ 5	0.4			5	0.64		0.51	1		0.36		mA
		0/10	0.5			10	1.6		1.3	2.6		0.9		
		0/15	1.5			15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/18	Any Input			18		± 0.1		$± 10^{-5}$	± 0.1		± 1	μA

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.
** Forced output disabled.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions					Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (V)	V_{CC} (V)	V_{DD} (V)	T_{Low}*		25 °C			T_{High}*		
								Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OH}, I_{OL}**	3-State Output Leakage Current		0/18	0/18			18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	µA
C_I	Input Capacitance			Any Input							5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20ns)

Symbol	Parameter	Shifting Mode	Test Conditions		Value			Unit
			V_{CC} (V)	V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time (data input to output) High to Low Level	L - H	5	10		300	600	ns
			5	15		220	440	
			10	15		180	360	
		H - L	10	5		850	1600	
			15	5		850	1600	
			15	10		290	580	
	Low to High Level	L - H	5	10		130	260	ns
			5	15		120	240	
			10	15		70	140	
		H - L	10	5		230	460	
			15	5		230	460	
			15	10		80	160	
t_{PHZ}	3-State Disable Delay Time Output High to High Impedance	L - H	5	10		60	120	ns
			5	15		50	100	
			10	15		35	70	
		H - L	10	5		120	240	
			15	5		120	240	
			15	10		40	80	
t_{PZH}	High Impedance to Output High	L - H	5	10		320	640	ns
			5	15		230	460	
			10	15		180	360	
		H - L	10	5		800	1500	
			15	5		800	1500	
			15	10		280	560	
t_{PLZ}	Output Low to High Impedance	L - H	5	10		370	740	ns
			5	15		300	600	
			10	15		250	500	
		H - L	10	5		850	1600	
			15	5		850	1600	
			15	10		350	700	